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PATENT DEPARTMENT
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AUSTIN, TX 78701-4039

EXAMINER

CLEARY, THOMAS J

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Serial No. : 09870447
Applicant : Brian Boles
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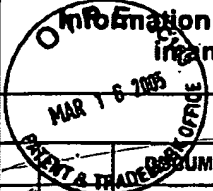
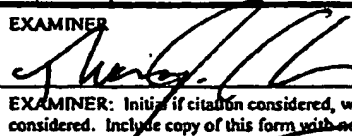
ACKNOWLEDGEMENT OF REQUEST

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The request for a copy of the initialed PTO 1449, dated December 10, 2004, has been received by the U.S. Patent and Trademark Office.

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SUNDA M. ARCHER
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PTO-1449		Application No. 09/870,447		Applicant(s) Brian Boles et al.			
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		U.S. PATENT DOCUMENTS					
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
TS A.	3930253	12/30/75	Maida	340	347	1/24/74	
TS B.	5974549	10/26/99	Golan	713	200	3/27/97	
TS C.	6055619	4/25/00	North et al.	713	36	2/7/97	
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TS E.	6728856	4/27/04	Grosbach et al.	711	202	6/1/01	
F.							
G.							
H.							
I.							
J.							
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	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
TS K.	01037424 A	2/89	JP	H03M	001/82		X
TS L.	0 554 917 A2	8/11/93	EP	G06F	9/26	X	
TS M.	0 855 643 A1	7/29/98	EP	G06F	9/30	X	
TS N.	0 992 888	12/4/00	EP	G06F	9/32	X	
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NON-PATENT DOCUMENTS							
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